International Journal of Electrical, Electronics and Mechanical Controls ISSN (Online) : 2319 – 7501

A Scientific and Scholarly Resource for Publication of Research Manuscripts

VOLUME 2 ISSUE 2 MAY 2013

Manuscript ID : ISSN23197501-V2I3M1-092013

Low Power High Speed 3-2 Compressor

Sanjeev Kumar[1], Manoj Kumar[2]

[1,2]Department of Electronics and Communication Engineering

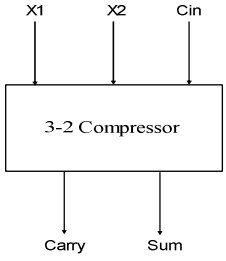
Guru Jambheshwar University of Science & Technology, Hisar, 125001, India

***Abstract*—** This paper describes a new design of low power 3-2 compressor circuit for high speed multipliers. Power consumption of proposed 3-2 compressor circuit varies from 0.355 nW to 1.6964 nW and delay varies from 2.0390 ns to 2.0224 ns. Further, power delay product of proposed circuit varies from 7.23×10^{-18}(J) to 34.30×10^{-18} (J) with varying supply voltage from 1.8V to 3.3V. The proposed compressor circuit shows better performance in terms of power consumption, output delay and PDP as compared to previous reported 3-2 compressor circuits. Simulation has been carried out using 0.18-µm CMOS technology.

***Index Terms*—** 3-2 compressor, CMOS, multiplier, power delay product.

1. INTRODUCTION

Multipliers are essential component in different circuits, particularly in arithmetic operation such as compressors, parity checkers and comparators. Multipliers consist of three fundamental parts: a partial product generator, a partial product reduction and a final fast adder part [1]-[4]. A booth encoder is used to generate the partial products and partial product are reduces to two rows using compressor circuits. Finally, fast adder is used to sum the two rows. The partial product reduction part of multiplier contributes maximum power consumption, delay and layout area. Various high speed multipliers use 3-2, 4-2 and 5-2 compressors to lower the latency of partial product reduction part [5]-[7]. These compressors are used to minimize delay and area which leads to increase the performance of the overall system. Compressors are generally designed by XOR-XNOR gates and multiplexers[8]-[11]. A compressor is a device which is used to reduce the operands while adding terms of partial products in multipliers. An X-Y compressor takes X equally weighted input bits and produces Y-bit binary number. The most widely and the simplest used compressor is the 3-2 compressor which is also known as a full adder [12]. A 3-2 compressor has three inputs X1, X2, X3 and generates two outputs, the sum and the carry bits. The block diagram of 3-2 compressor is shown in figure 1.



(a)

X1	X2	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(b)

Figure 1: (a) A 3-2 compressor (b) 3-2 compressor truth table

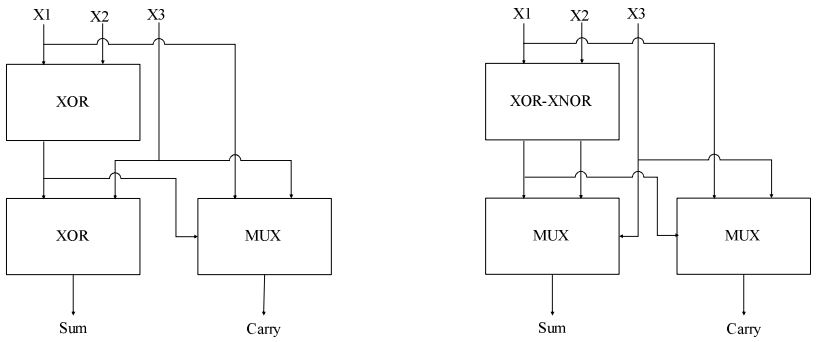
International Journal of Electrical, Electronics and Mechanical Controls ISSN (Online) : 2319 – 7501
A Scientific and Scholarly Resource for Publication of Research Manuscripts

VOLUME 2 ISSUE 2 MAY 2013

Manuscript ID : ISSN23197501-V2I3M1-092013

A 3-2 compressor cell can be implemented in many different logic structures. However, in general, it is composed by three main modules. The first module is required to generate XOR or XNOR function, or both of them. The second module is used to generate sum and the last module is to produce carry output. The 3-2 compressor can also be implemented as full adder cell when its third input is taken as the Carry input from the preceding compressor block or X3 = C_{in}. The basic equation of 3-2 compressor is:

$$X1 + X2 + X3 = Sum + 2 \bullet Carry \quad (1)$$



(a) **(b)**

Figure 2: (a) Conventional 3-2 compressor (b) Improved 3-2 Compressor architecture

The conventional architectures of 3-2 compressor shown in figure 2(a), it has two XOR gates in the critical path. The sum output is generated by the second XOR and carry output is generated by the multiplexer (MUX). The equations governing the conventional 3-2 compressor outputs are shown below:

$$Sum = X1 \oplus X2 \oplus X3 \quad (2)$$

$$Carry = (X1 \oplus X2) \bullet X3 + \overline{(X1 \oplus X2)} \bullet X1 \quad (3)$$

The 3-2 compressor architecture shown in figure 2(b) has less delay as compared to other architectures, as some of the XOR circuits are replaced by the multiplexer circuits. In this compressor the select bit at multiplexer present before the input arrives, so reduces the delay. Thus the switching time of the transistors in the critical path is decreased [5]. This minimizes the delay to a significant amount. This architecture shows critical path delay of Δ-XOR +Δ-MUX. Output functions of modified 3-2 compressor circuit are shown by the equations as given:

$$Sum = (X1 \oplus X2) \bullet \overline{X3} + \overline{(X1 \oplus X2)} \bullet X3 \quad (4)$$

$$Carry = (X1 \oplus X2) \bullet X3 + \overline{(X1 \oplus X2)} \bullet X1 \quad (5)$$

In this paper, we propose an improved design of 3-2 compressor based on a new XOR-XNOR module. The rest of paper is organised as follows: In section II describes the some previously reported 3-2 compressor circuits. In sections III new 3-2 compressor is presented. In section IV results have been obtained and compared with previous reported circuits. Further, conclusions are presented in section IV.

International Journal of Electrical, Electronics and Mechanical Controls ISSN (Online) : 2319 – 7501
A Scientific and Scholarly Resource for Publication of Research Manuscripts

VOLUME 2 ISSUE 2 MAY 2013

Manuscript ID : ISSN23197501-V2I3M1-092013

2. PREVIOUS WORK

Various 3-2 compressor circuits have been reported in literature. A modified architecture of 3-2 compressor as shown in figure 2(b) is reported in [5]. The designed 3-2 compressor has been implemented with one XOR-XNOR and two multiplexer modules as shown in figure 3. This circuit has higher delay and requires large area due to more numbers of transistors. Another, 3-2 compressor using ten transistor XOR-XNOR modules is reported in [6]. In this design, two pull-up PMOS transistors and two pull-down NMOS transistors are added to restore full swing operation. This circuit shows poor performance when cascaded. Multiplexer based on transmission gates have been used with output buffer which improves the driving capability but increase its power dissipation. Figure 4 shows the transistor level implementation of 3-2 compressor [6].

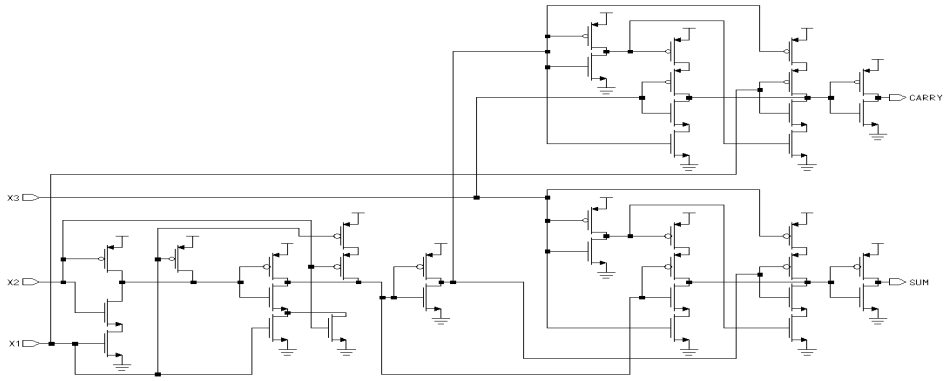


Figure 3: 3-2 Compressor [5]

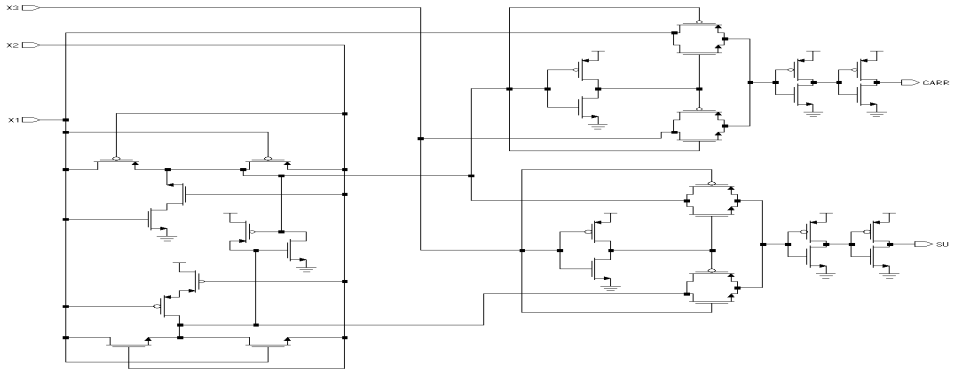


Figure 4: 3-2 Compressor [6]

3. PROPOSED WORK

International Journal of Electrical, Electronics and Mechanical Controls ISSN (Online) : 2319 – 7501
A Scientific and Scholarly Resource for Publication of Research Manuscripts

VOLUME 2 ISSUE 2 MAY 2013

Manuscript ID : ISSN23197501-V2I3M1-092013

The proposed 3-2 compressor has been designed with the new XOR-XNOR module with eight transistors and transmission gate 2-1 multiplexer without the output buffers. This multiplexer design is faster and dissipates low power than the standard CMOS design. Gate lengths of all the transistors have been taken as 0.18µm. Width (*Wp*) for PMOS transistors have been taken as 1.2µm. Widths (*W*n) of NMOS transistors have been taken as 0.6µm. The modified architecture of 3-2 Compressor shown in figure 2(b) has been used for the implementation of proposed 3-2 compressor circuit in which one XOR-XNOR and two multiplexers are used. The sum and carry outputs are generated with the transmission gate multiplexer circuits. The complete circuit diagram of proposed 3-2 compressor is shown in figure 5.

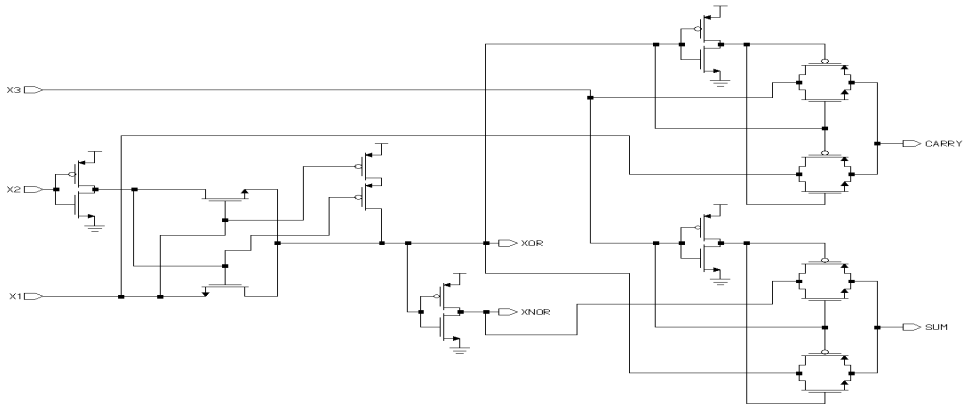


Figure 5: Proposed 3-2 compressor circuit

4. RESULTS AND DISCUSSIONS

Simulations have been performed using TSMC 0.18µm CMOS technology at 100 MHz frequency. The power consumption results of proposed and previous reported 3-2 compressor circuits with variation in supply voltage from 1.8V to 3.3V shown in table 1.

Table 1: Power consumption of 3-2 compressor circuits

Supply Voltage (V)	Power consumption (nW)		
	Ref. [5]	Ref. [6]	Proposed circuit
1.8	0.429	0.383	0.355
2.0	0.544	0.496	0.455
2.2	0.681	0.634	0.574
2.4	0.838	0.798	0.714
2.6	1.0229	1.0015	0.879
2.8	1.2349	1.2289	1.0709
3.0	1.4796	1.5051	1.2941

International Journal of Electrical, Electronics and Mechanical Controls ISSN (Online) : 2319 – 7501
A Scientific and Scholarly Resource for Publication of Research Manuscripts

VOLUME 2 ISSUE 2 MAY 2013

Manuscript ID : ISSN23197501-V2I3M1-092013

3.3	1.9155	2.0156	1.6964

Table 2: Delay of 3-2 compressor circuits

Supply Voltage (V)	Maximum output delay (ns)		
	Ref. [5]	Ref. [6]	Proposed circuit
1.8	2.0873	2.0879	2.0390
2.0	2.0770	2.0777	2.0347
2.2	2.0697	2.0693	2.0313
2.4	2.0646	2.0640	2.0287
2.6	2.0606	2.0595	2.0267
2.8	2.0572	2.0561	2.0252
3.0	2.0547	2.0532	2.0239
3.3	2.0521	2.0500	2.0224

Table 3: Power delay product (PDP) of 3-2 compressor circuits

Supply Voltage (V)	PDP × 10^{-18}(J)		
	Ref. [5]	Ref. [6]	Proposed circuit
1.8	8.95	7.99	7.23
2.0	11.29	10.35	9.25
2.2	14.09	13.11	11.65
2.4	17.30	16.47	14.48
2.6	21.07	20.62	17.81
2.8	25.40	25.26	21.68
3.0	30.40	30.90	26.19
3.3	39.30	41.31	34.30

International Journal of Electrical, Electronics and Mechanical Controls ISSN (Online) : 2319 – 7501
A Scientific and Scholarly Resource for Publication of Research Manuscripts

VOLUME 2 ISSUE 2 MAY 2013

Manuscript ID : ISSN23197501-V2I3M1-092013

Power consumption of proposed 3-2 compressor circuit varies from 0.355 nW to 1.6964 nW with change in supply voltage from 1.8V to 3.3V. Table 2 shows comparison of maximum output delay of proposed and earlier reported circuits with varying supply voltage from 1.8V to 3.3V. Proposed 3-2 compressor circuit shows delay variation from 2.0390 ns to 2.0224 ns. Further, table 3 compares the power delay product (PDP) of 3-2 compressor circuits. PDP of proposed circuit varies from 7.23×10^{-18}(J) to 34.30×10^{-18} (J). Input and output waveform results for proposed 3-2 compressor at 3.3 V are shown in figure 6.

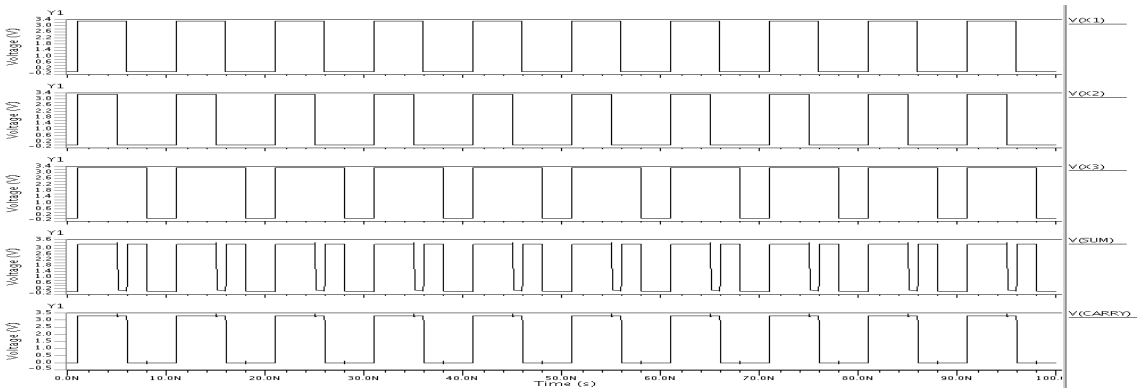
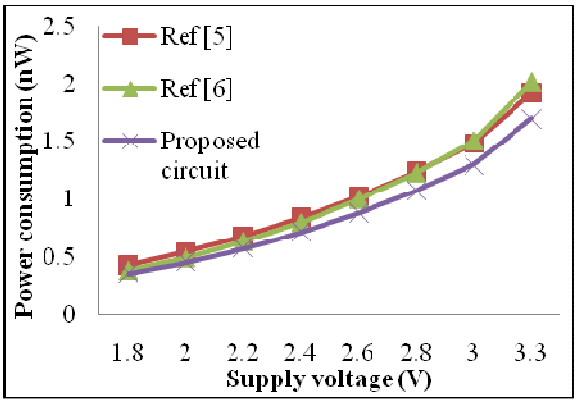
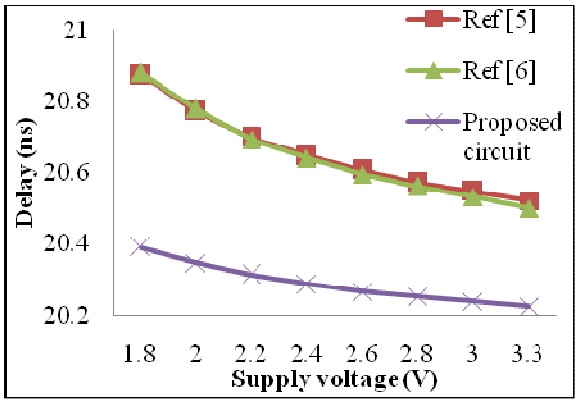


Figure 6: Input and output waveform results for proposed 3-2 compressor at 3.3 V



(a)

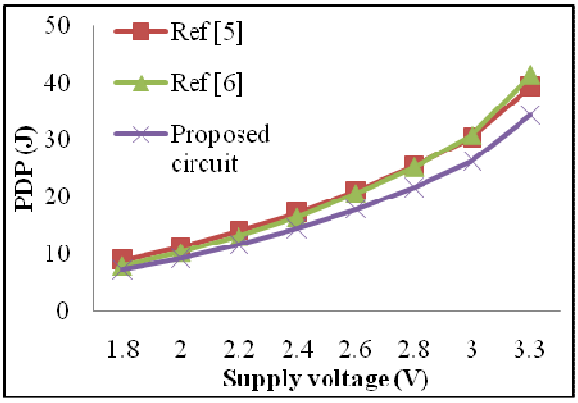


(b)

International Journal of Electrical, Electronics and Mechanical Controls ISSN (Online) : 2319 – 7501
A Scientific and Scholarly Resource for Publication of Research Manuscripts

VOLUME 2 ISSUE 2 MAY 2013

Manuscript ID : ISSN23197501-V2I3M1-092013



(c)

Figure 7: (a) Power consumption (b) Output delay (c) PDP of 3-2 compressor circuits

Figure 7(a) show comparison of power consumption with variation in supply voltage for different compressor circuits. It has been observed that power consumption of proposed 3-2 compressor circuit is lowest among the compared circuits. Figure 7(b) compares the maximum output delay of proposed and earlier reported 3-2 compressor circuits. Further, power delay product (PDP) comparison has been shown in figure 7(c) and it has been observed that the PDP of proposed 3-2 compressor is least among these circuits. Therefore, the proposed compressor achieves improved performance.

5. CONCLUSIONS

In this paper, a new 3-2 compressor circuit has been reported. The compressor shows minimum power consumption of 0.355 nW with supply voltage of 1.8V. Maximum output delay of compressor is 2.0390 ns with supply voltage of 1.8V. Further, circuit shows PDP of 7.23×10^{-18}(J) at supply voltage of 1.8 V. The performance of the 3-2 compressor is compared and the simulation results proved that proposed 3-2 compressor has low power consumption and lowest PDP.

REFERENCES

[1] K. Prasad, K.K. Parhi, "Low power 4-2 and 5-2 compressors," *Proceedings of 35th Asilomar Conference on Signals, Systems and Computers*, Vol. 1, pp. 129-133, 2001.

[2] Z. Wang, G. A. Jullien, and W. C. Miller, "A new design technique for column compression multipliers," *IEEE Trans. Comput*., vol. 44, pp. 962–970, Aug. 1995.

[3] S. F. Hsiao, M. R. Jiang, and J. S. Yeh, "Design of high speed low-power 3-2 counter and 4-2 compressor for fast multipliers," *Electron. Lett,* vol. 34, no. 4, pp. 341–343,1998.

[4] Kwon, O., Nowka, K., and Swartzlander, E.E. "A 16-bit x 16-bit MAC design using fast 5:2 compressor," *Proc. IEEE Int. Conf. on Application-Specific Systems, Architectures, and Processors*, pp. 235–243, 2000.

[5] S. Veeramachaneni, K. M. Krishna, L. Avinash, S. R. Puppala, and M. Srinivas, "Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors," in *VLSI Design, 2007. Held jointly with 6th*

International Journal of Electrical, Electronics and Mechanical Controls ISSN (Online) : 2319 – 7501
A Scientific and Scholarly Resource for Publication of Research Manuscripts

VOLUME 2 ISSUE 2 MAY 2013

Manuscript ID : ISSN23197501-V2I3M1-092013

International Conference on Embedded Systems., 20th International Conference on, pp. 324–329, Jan. 2007.

[6] Jorge Tonfat, Ricardo Reis, "Low Power 3-2 and 4-2 Adder Compressors Implemented Using ASTRAN", *IEEE Third Latin American Symposium on Circuits and Systems* (LASCAS), Feb. 29, March 2, 2012.

[7] C. H. Chang, J. Gu, M. Zhang, "Ultra low-voltage low power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits," *IEEE Transactions on Circuits and Systems*, vol. 51, issue 10, pp. 1985 – 1997, Oct. 2004.

[8] Manoj Kumar, Sandeep K. Arya, Sujata Pandey, "Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate," *International Journal of VLSI design & Communication Systems*, vol. 2, pp. 47-59, 2011.

[9] D. Radhakrishnan, A.P. Preethy, "Low Power CMOS pass logic 4-2 compressor for high speed multiplication", Proceedings of 43rd *IEEE Midwest Symposium on Circuits and Systems*, vol. 3, pp. 1296-1298, 2000.

[10] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid- State Circuits*, vol. 32, pp. 1079–1090, July 1997.

[11] Manoj Kumar, Sandeep K. Arya, and Sujata Pandey, "A New Low Power Single Bit Full Adder Design with 14 Transistors using Novel 3 Transistors XOR Gate," *International Journal of Modeling and Optimization*, Vol. 2, No. 4, pp. 544-548, August 2012.

[12] Nilay Nagdeve, Vishal Moyal, Ms. Archana Fande, "A Simulation Based Evaluation of Different Compressors for Fast Multiplication," *International Journal of Scientific & Engineering Research,* vol. 3, issue 6, June 2012.